AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 3, line 16, as follows:

To the contrary, when a resist pattern has a broad dimensional margin in which a semiconductor integrated circuit can properly operate, it is not necessary to determine a [[sever]]severe test standard. This is because a [[sever]]severe test standard causes an increase in repair of a mask pattern with the result of an increase in a turn-around time (TAT) for fabricating a mask.

Please amend the paragraph beginning at page 15, line 27, as follows:

By selecting the sampling points 15X, 16AX, 16BX, 17X and 17Y in the above-mentioned manner, it is possible to appropriately select the sampling points in accordance with a structure of a semiconductor integrated circuit as a final product. For instance, dimensions of an area in which a contact makes contact with a wiring formed in a gate wiring layer, and an area around the area (namely, the contact area 21) in the designed pattern 11 have to be accurately tested in order to ensure electrical connection in a semiconductor integrated circuit. Furthermore, in order to have a MOS transistor in a semiconductor integrated circuit ~~accomplished~~ accomplish desired performances, dimensions of a portion acting as a gate of a MOS transistor and an are around the portion (namely, the field layer area 22) in the designed pattern 11 have to be accurately tested. On the other hand, the rest of a gate wiring layer does not exert [[a]]as much influence on behavior of a semiconductor integrated circuit, and hence, it is not necessary to accurately test the rest of a gate wiring layer.

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